DESIGN OF POWER DROOP REDUCTION IN SEQUENTIAL CIRCUITS WITH SCAN BASED BIST

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ABSTRACT

Testing is an essential domain in vlsi circuits design.Test power has been turned as a bottleneck for testing. serious negative effects of excessive power dissipation,speed and area are considered during testing. The scan-based testing not only elevates power consumption but also introduces speed in the combinational logic. Low power testing is used to overcome drawbacks of scan based testing. In this project, scan based BIST(Built In Self -Test) is used but previous scan testing has a power droop problem. power droop is a speed control mode.This problem is reduced during a speed test of sequential circuits with scan-based BIST. The LFSR is used to implement the test pattern for detecting faults. This project introduces a ISCAS '85 benchmark circuits for speed testing.The proper modification of test vectors is used to reduce a power droop problem and also reduces a area .As a result, low power and high fault coverage is achieved. The design has been coded in verilog. The simulation results has been viewed by Modelsim software and Quartus II software. The obtained simulation results is used for industrial applications.

Keywords: *Built In Self Test; Pseudo Random Test Pattern Generator; Linear Feedback Shift Register*

; I. INTRODUCTION

The new domain of computing was ushered in by multiple advancements in electronic miniaturization and the semiconductor transistor by Bardeen in 1947-48, and then the Bipolar Transistor by Shockley in 1949. Since the invention of the first Integrated Circuit(IC) by Jack Kilby in 1958, our ability to pack more and more transistors onto a single chip has been very rapid. In the early 1960s, low density fabrication processes classified under Small Scale Integration (SSI) in which transistor count was limited to about 10. This rapidly gave way to Medium Scale Integration (MSI) later in the decade, when around 100 transistors could be placed on a single chip. Declining costs of research encouraged private companies to enter the industry in contrast to the earlier years where the main burden was borne by the military[2].

Early 1970s[3] saw the growth of transistor count to about 1000 per chip called the Large Scale Integration (LSI). By mid-1980, the transistor count on a single chip exceeded 1000 and hence came the age of Very Large Scale Integration or VLSI, which is large scale integration with a single chip of size as small as 50 millimeters square having more than a million transistors and circuits in it.

In vlsi circuits design,Testing is an important domain. Testing assures that the function of each manufactured circuit corresponds to the function of the implementation. Basic types of defects in VLSI circuits are the following: particles (small bits of material that bridge two lines), incorrect spacing, incorrect implant value, misalignment, holes (exposed area that is unexpectedly etched), weak oxides, and contamination.

Testing has a internal testing(BIST)[1] which is classified as 2 types[2] such as scan based testing and low power testing. BIST is the capability of the circuit to test itself. BIST techniques are used to find the faults in a circuit design and also reduced the difficulty in VLSI testing. A logic BIST controller is used to control the BIST operation. The test pattern generator (TPG) automatically generates test patterns that are applied to the inputs of the circuit under test (CUT) and test response analyzer (TRA[9]) is used for compacting the circuit's output responses.

The scaling is an important factor for IC fabrication technology. This is performed a serious effects of

testing and reliability.In IC fabrication,usage of test vectors are higher than the field operation. Consequently, excessive power droop (PD) may be

Scan[4] is used to testing a sequential circuits in a efficient manner. Low power design is the major design objective which is widely used for communication ,signal processing and IC fabrication technology.Low power testing may be measured with the switching activity of the scan cells Previous method is considered about a testing of scan chains.As a result,power droop problem is occurs .To overcome this problem,Reduction of power droop (PD) during at-speed test of sequential circuits with scan-based BIST Scheme is proposed.

II. PREVIOUS WORK

Scan chain segmentation with gated clocking[5] is used to reduce capture power. The proposed methods divide the scan chains into several segments, enabling only one scan chain segment at a time to capture the test responses. This reduces the number of gates in combinational logic as well as switching activity.but it cannot consider that power droop problem.

In previous methods,[9]A new low-power (LP) scan-based BIST technique is proposed based on weighted pseudo random test pattern generation and reseeding. This project has a LP (low power) Weighted pseudo random test pattern generator (PRPG) which has the capacity to produce the pseudo random test pattern generator with reseeding. LP (low- power) reseeding techniques are used to create a feedback for high accuracy and also cover all test vectors. In both techniques, only a small number of flip flops can activated.This paper reduces a power and area but it cannot achieve a speed strategy.

In previous method[8], test pattern generator with a pre-selected toggling level (PRESTO) is presented. This is a successful approach to reduce PD at capture in scan-based LBIST employing the LOS scheme. But it cannot achieve a test time,test volume and power .

In speed test[11], PD at capture is reduced by a multi-cycle BIST scheme with partial observation. but enables to reduce PD at capture only during scan-based LBIST employing the LOC scheme.it does not a enables in shift cycle for reduce a power droop.

In speed tes[12]t, an effective method to generate test patterns such that the switching activity during capture cycles of the tests is low but power droop problem is occurs. The proposed method uses generated, which will slow down the circuit under test (CUT) signal transitions[8].As a result ,delay fault will occurs.

background states obtained by applying a number of functional clock cycles .

In power droop testing[10],we propose an automatic test pattern generation (ATPG) algorithm which attempts to create worst-case power droop conditions by combining the effects of low-frequency and high-frequency power droop.

To overcome this problem,sequential circuit testing is used.In our method, we propose a novel approach to reduce PD during the application of test vectors, thus reducing the probability of generating false test fails during test, in scan based LBIST employing the Launch On Shift scheme.and also reduced a test vectors as well as get a high fault coverage .The phase shifter drives a all test vectors at a time.It depends on present and future test vectors.As a result,tester time and power will be reduced.

III.PROPOSED WORK

The proposed method based on four efficient techniques such as,

- Scan based BIST
- Power droop strategy
- Shift and capture scheme
- Sequential circuit testing with extra variable injection algorithm

1)Scan based bist

.In earlier days, automatic test equipment is used for pattern generation .Due to high cost and high switching activity ,scan based BIST[3] is introduced .It is classified as two types,

- Memory based BIST
- Logic based BIST

In both cases, a linear feedback shift register (LFSR) generates the test vectors that are given to the CUT.Circuit Under Test(CUT) [6]is based on either combinational circuits and sequential circuits.In memory based bist,D flipflops is used for testing.but it has a power droop and power dissipation during a shift and capture phases and The phase shifter depends on present test vectors.so,tester time and volume increased as well as area should be increased.To overcome this problem,Logic based bist is used.Logic based bist performs a circuit testing in a efficient manner. Scan based at-speed testing has become mandatory in industry to detect delay defects today in order to maintain test quality and reduce test cost.

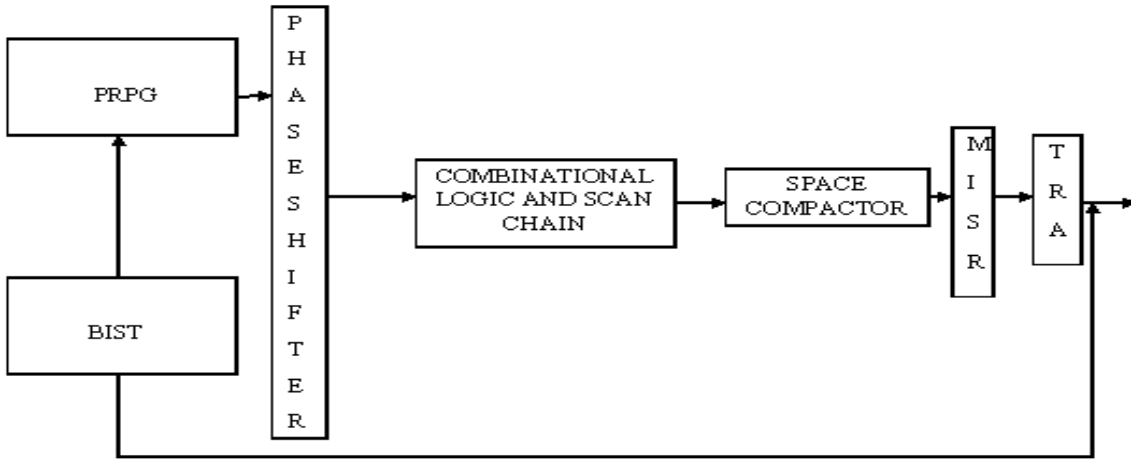

Fig 1: Basic structure of scan based bist

Fig 1 shows a structure of scan based bist.BIST is give the test vectors to PRPG.LFSR pattern implemented in PRPG. The Phase Shifter (PS)[2] is used to shift and capture the test vectors .usually, LFSR pattern is smaller than the scan chains. At the same clock cycle, the PS provides as outputs, the current LFSR sequence together with many future/past sequences. In our proposed solution , derive the new test vectors allowing to reduce PD during capture cycles.The Space Compactor compacts the outputs of the scan chains and to match the input as well as output by MISR. This test vectors applied to Test Response Analyzer for getting a desired output.

2)Power droop strategy

Power droop[6-8] is a power integrity condition and speed control mode. It arises under specific conditions ,power dissipation and leads to fails in circuit operation. If power droop is not identified, it affects a whole field operation . if power droop is identified, the parts of the design which need improvements are determined easily. Consequently, increasing a power droop(PD) during at-speed test may take place. This causes the occurrence of delayed transitions of signals of the circuit under test (CUT), which may be erroneously recognized as the presence of delay faults. As a result, test will fails. Thus , increases yield loss and tester time.

In fabrication process[9-12],we consider that power droop problem.

• How many droop inducers should be inserted in the design and where should they be placed?

• The amount of reducing/increasing droop level is test pattern dependent. It is based on the switching activity.

• It is not a solution to deal with the voltage droop that fails the scan shift operation ,It is only applicable for capture power.

These are the impact factors of power droop problem[7]. Power-aware ATPG tends to reduce the capture power as much as possible to reduce a switching activity.

3)Shift and capture scheme

Shift and capture scheme [4]is widely performed by phase shifter. phase shifter can controls a whole test vectors ,In our method ,phase shifter based on present and past, future test vectors for reducing a power droop problem. In case of power droop, power dissipation will occurs. If reducing a power droop ,we can minimize a test power during testing. Test power is classified as four different types,

- Scan-in power
- Scan-out power
- Scan Capture power
- Scan Shift power

Scan[10] in power is nothing but total power consumption of test vectors during scanning process. scan out power is nothing but total power consumption of captured test vectors during scanning process. scan shift power is a combination of scan in and scan out power. Capture power is nothing but instantaneous power consumed

In scan based BIST, two basic schemes are used.

- Launch on shift(LOS)
- Launch on capture(LOC)

In LOS[11], the test vectors are applied to the CUT at the last shift cycle of the shift phase, and the CUT response is sampled on the scan chains at the following capture cycle. In the LOC scheme, the test vectors are first loaded into the scan-chains during the shift-phase, then, in the following capture phase the test vectors are applied to the CUT, and the CUT response is captured on the scan chains at two following capture cycles.

In this paper[8] , we consider scan-based BIST based on LOC and LOS for high performance microprocessors. During a LOC and LOS, delay effect can be erroneously recognized as caused by a delay fault, with the consequent generation of a false test fail. If reduce a test vectors in shift and capture phases, we can reduce a power droop .In this case,The Phase shifter provides the previous and future test vectors for all scan-chains. As a result, test vectors decreased .it can able to achieve a high fault coverage.

4)Sequential circuit testing with extra variable injection algorithm

Testing is an important factor for manufacturing process.It is classified into two different types based on the circuit.

- Combinational circuit testing
- Sequential circuit testing

Due to switching activity,area,and power droop problem,sequential circuit testing is used.Usually,sequential circuit is a combination of combinational circuit and flipflops.The proposed system [11-12]based on the reduction of Power droop[12] that may generate false test fails during speed test with scan-based BIST .Instead of flipflops, sequential circuits is to be tested.In this case,above drawbacks can be reduced by proposed method.

Fig 2 shows a sequential circuit testing[1-5].In this architecture, BIST controller is used to send a test vectors to LFSR and MUX .The test vectors are enabled for scan a sequential circuit by using MUX. LFSR is used to generate a test pattern for given test vectors.Extra variable is injected to the test vectors for identifying the faults in a circuit. Each stage of the PS drives multiple scan chain instead of a single scan chain, while each stage of the PS requires a few number of XOR gates. As a result, test vectors are reduced. CUT is used to compare the LFSR pattern and after scanning pattern. These test patterns of test vectors are given to the MISR. Output response is kept in MISR. Again, this test vectors are feed to the BIST controller for detects faults.

Fig 3[1] shows a combination of ISCAS '85 benchmark circuits and D flipflops. ISCAS '85 benchmark circuits are ten combinational networks provided to authors at the 1985 International Symposium on Circuits And Systems. They subsequently have been used by many researchers as a basis for comparing results in the area of test generation.The ISCAS '85 benchmark circuits are,c1, c5, c17, c432, c499, c880, c1355, c1908, c2670, c3540.In this case,C17 CIRCUIT is used.

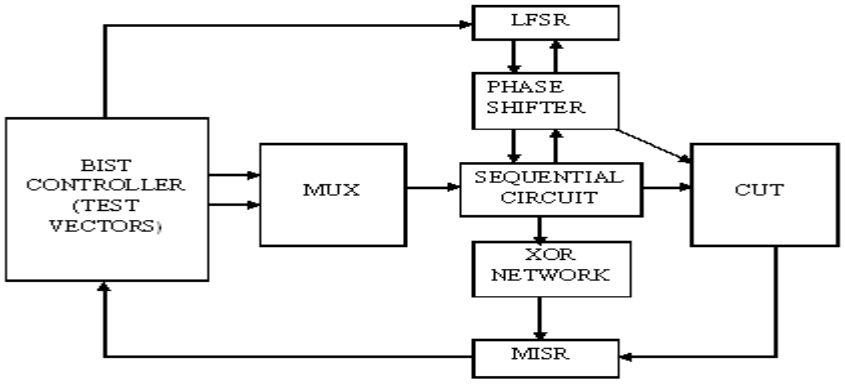

Fig 2:General DFT architecture for sequential circuit testing

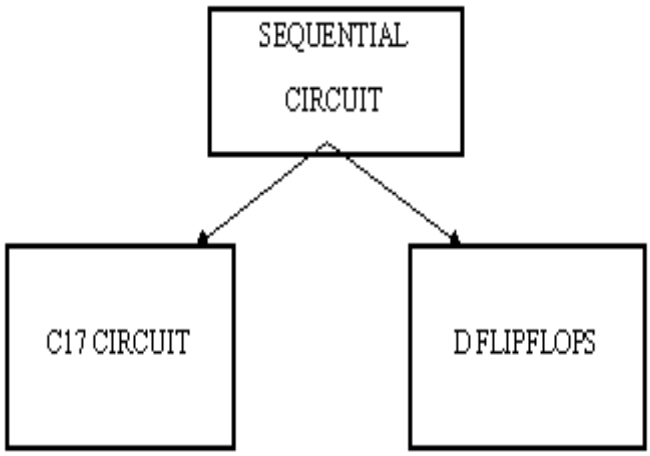

Fig 3:Basic sequential circuit testing

IV.RESULTS AND DISCUSSION

The approach of scan based BIST is validated by four modes of operation. The operations are

(i) Idle mode

(ii) Reset mode mode

(iii) Pattern check mode (extra variable injection algorithm)

(iv)Power droop reduction mode.

1)Idle mode

In Idle mode, clock, reset and test does not produced.Result shows that desired test pattern is calculated (Fig. 2). In this wave form, three states are used such as clock, reset, and test. Depending on these three states, we can detect faults in a circuit. 16 bit sequence of test vectors is used and this vectors applied to scan chain to reduced area, power droop and power dissipation and tester time.

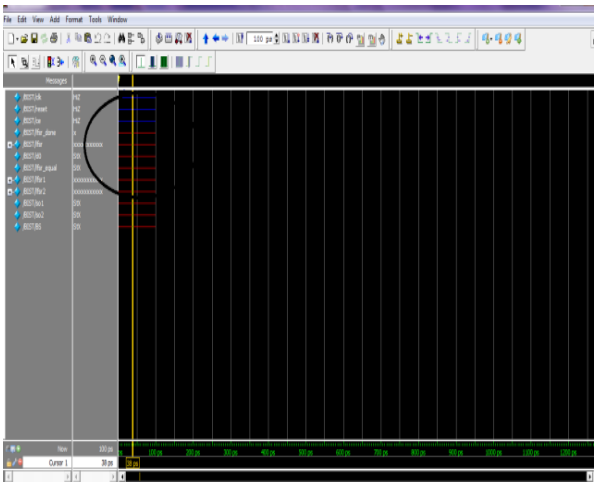

Fig 4:Test pattern for idle mode

2)Reset mode

After idle mode,reset mode will be activated.In this mode,assigning a value of clock,reset and test.The value of clock is clock and reset is enable that is one .and test is enable .If reset mode ,BIST control and generation of test vectors are enabled.During the testing process,the test vectors are automatically generates a test pattern in a effective manner.In this case,pseudo random test pattern generation is used for random pattern creation.

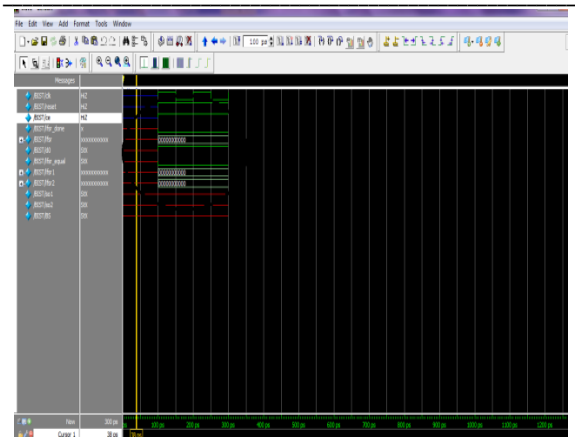

Fig 5:Test pattern for reset mode

3)Pattern check mode for extra variable injection algorithm

In Pattern check mode,reset will be zero .As a result,test vectors are generated without increasing a area constraints. Extra variable injected to test vectors. That means fault is occurs. 16 bit test vectors continuously processed for detects a faults.

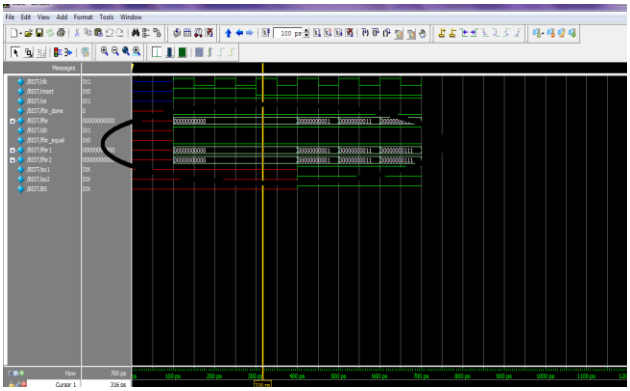

Fig 6:Test pattern for pattern check mode

4)Power droop reduction mode

Power droop reduction mode is nothing but BIST valid mode.BIST valid mode has 2 outputs for LFSR pattern due to C17 circuit testing. If output is high, fault will be detected otherwise no fault is occurred in testing process.power droop is a speed control mode.In this mode,output is quickly responsed.As a result speed is increased and power droop is reduced.By a proper modification of test vectors area should be minimized as well as switching activity and power dissipation is reduced.

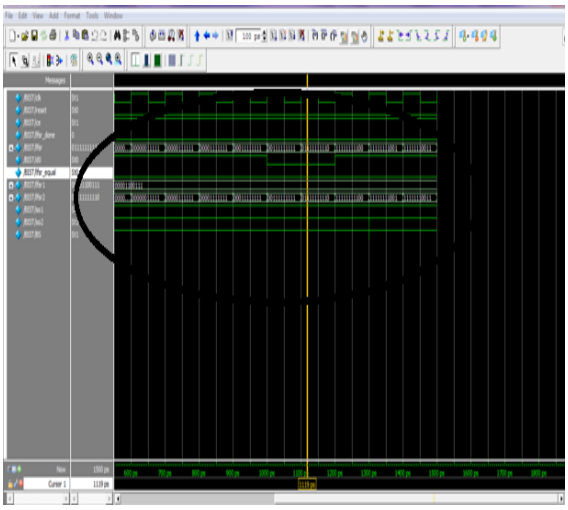

Fig 7:Test pattern for power droop reduction mode

TABLE 1.POWER, AREA, TEST TIME COMPARISON OF SCAN BASED BIST

S.NO	PARAMETERS	EXISTING	PROPOSED
1.	POWER	34.47mW	31mW
2.	AREA EFFICIENCY	28%	53%
3.	RUN TIME	4.451ns	0.654ns

The proposed design is compared with previous scan based designs in terms of area, power and speed. After simulation, using Quartus –II software I have analysed these three parameters for both the cases. As the numbers of test vectors are reduced in proposed design comparing to earliest one, the power droop and area are significantly reduced. From above table,we analysed that run time is decreased by 3mW .

V.CONCLUSIONS

Thus, The BIST architecture proposed is implemented using Verilog language and tested on various faulty circuits. Then design has been synthesized on fault has been created and simulated on Modelsim software and power, area, speed has been analysed by Quartus II power analyser tool. In this paper,A novel approach to reduce the power droop (PD) during speed test of sequential circuits with scan-based BIST Scheme is proposed.. The proposed solution enables designers to reduce the probability that the delay induced by PD exhibited during at-speed test is erroneously interpreted as a delay fault,with consequent generation of a false test fail .our approach allows us to achieve a scalable PD reduction with no drawback on the required number of test vectors to achieve a target FC. It has been used to reduce a power, speed, area for a different set of useful test vectors is to be selected from the random sequence, or the scan path architecture is to be radically redesigned. Experimental results have demonstrated the performance of the proposed method by comparision with a recent BIST method[1-12]..

CONFLICT OF INTEREST

No conflict of interest

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