A DESIGN OF 0.18µm SUBTHRESHOLD 7T NON VOLATILE SRAM BIT CELL

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Abstract - On-chip cache memories are present in every system on chip devices. These cache memories are made up of static random access memory (SRAM). Low power and High speed are the constraints placed on the SRAM cell design. The increased importance of lowering power in memory design has produced a trend for operating memories at lower supply voltages. The implementation of conventional 6T SRAM memory is scaling to newer technology as it operated in the deep submicrometer region has become difficult due to the compromise between area, power, and performance. To overcome the read-write conflicts 7T cell is proposed. The 7T cell is operated at the 0.4v and can also achieve the low area per bit cell by using 0.18µm Technology. The 7T static random access memory has improved read and write stability and noise margin free read operation also in the sub-threshold region.

Keywords-Cache memory, Low power, Seven-transistor(7T) Static random access memory(SRAM), Subthreshold (ST), Noise margin.

I. INTRODUCTION

Semiconductor Electronics has significantly dominated the Industry as well as the domestic side. Along with the advancements in microelectronic technology, revolutionary changes have taken place in a short span of time. On recent deep sub-micrometer technology nodes, the scaling of transistors in digital design to decrease power and improve performance has become a significant challenge. With the decrease in technology node, the circuits become more vulnerable to variability and noise.

Due to the energy constraints of battery-powered devices, research in low power consumption circuits has become more imperative than ever before. Hence the supply voltage is scaled to decrease power consumption, it has been a popular choice due to its effect on quadratic reduction in power. It can perform well in subthreshold (ST) and near-threshold applications, which attempt to reach the minimum energy point to save power but pose challenges like increased susceptibility to noise and loss in performance.

Moore's law which predicts that the chip density is the prime force behind the advancements of VLSI design. Complementary Metal Oxide Semiconductor circuits are preferred in most of the VLSI design compared to Bipolar. The advantage of CMOS technology is the scalability and ability to shrink in size. Static Random Access Memories are the predominant technologies used to implement memory cells. SRAM cache influence the system speed and power consumption in a modern computer system. The SRAM parameter variations dominate the overall circuit parameter characteristics as more and more area is dedicated to memory in the forthcoming generations. Therefore, a deep knowledge and analysis about the stability of the SRAM cells is a must.

A. SUBTHRESHOLD OPERATION

The digital circuit design operated in the sub-threshold region has emerged as a low energy solution for applications with strict energy constraints. Analysis of sub-threshold designs has focused on logic circuits for example, SRAMs comprise a significant percentage of the total area for many digital chips as well as the total power. For this reason, SRAM leakage can dominate the overall leakage of the chip, and largely switched capacitances in the bit lines and word lines make SRAM accesses costly in terms of energy.

The performance of SRAM operation into the sub-threshold region reduces both leakage power and access energy. It is also used for system integration, SRAM must become capable of operating at sub-threshold voltages that are compatible with sub-threshold combinational logic. Recent low power memories show a trend of lower voltages with some designs holding state on the edge of the sub-threshold region and these scaling

promises to continue, leading to sub-threshold storage modes and even sub-threshold operation for SRAMs operating in tandem with sub-threshold logic.

II. LITERATURE SURVEY

A typical conventional six-transistor SRAM cell in a 180nm CMOS technology is shown in Fig. 1. The robustness of an SRAM cell is characterized by its hold stability during a read operation. In a conventional 6T SRAM cell, the data storage nodes are directly accessed through the pass transistors connected to the bit lines. The storage nodes are disturbed due to the voltage division between the cross-coupled inverters and the access transistors during a read operation. The data is most vulnerable to external noise during a read operation due to this intrinsic disturbance produced by the direct data-read-access mechanism of a standard 6T SRAM circuit (destructive read).

There are strict constraints on the sizing of transistors to be able to maintain the data stability and functionality of a standard6T SRAM cell. The design of a 6T SRAM cell is typically characterized by the ratio (β) of the size of the pull-down transistors to the access transistors. In order to maintain the read stability, N1 and N2 (Fig. 1) must be stronger as compared to the access transistors N3 and N4. Alternatively, for writeability, N3 and N4 must be stronger as compared to P1 and P2.These requirements are satisfied with careful transistor sizing, as illustrated in Fig.1.In addition to the data stability issues, the increasing leakage energy consumption of the embedded memory circuits is also a growing concern. In modern high-performance microprocessors, more than 40% of the total active mode energy is consumed due to leakage currents. As more transistors are integrated on a die with each new technology generation, leakage energy will soon dominate the total active mode energy consumption. Furthermore, leakage is the only source of energy consumption in an idle circuit.

Memory arrays are an important source of leakage since the majority of transistors are utilized for on-chip caches in today's high-performance microprocessors. The design of a low leakage SRAM cell with enhanced data stability is, therefore, highly desirable. The SRAM array has been the industry standard due to its fast differential sensing and very low area. However, the extensive scaling of supply voltage has affected

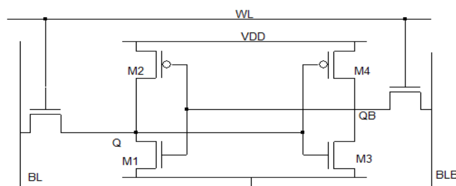


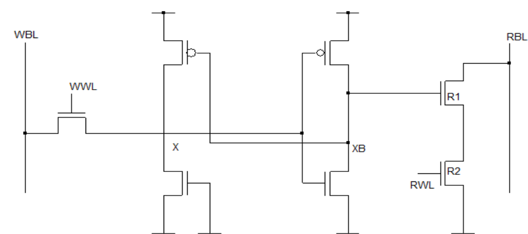
Fig.1. Conventional 6T SRAM Cell

the performance of the read and write operations in SRAMs, thereby making it difficult to implement the conventional 6T cell.

Although at strong inversion, device sizing is enough to ensure proper functioning of the memory cell, at low voltages (weak inversion), process-voltage-temperature(PVT) variations and local mismatch cause the memory to malfunction. Many structures have been proposed to solve this problem. The decoupling of the read and write ports to have a read static noise-margin (RSNM)-free read, as in the seven-transistor (7T) and eight-transistor (8T) cell has been a viable approach to improve noise margins but it comes at the expense of increased area and degraded read performance due to single-ended sensing. Such single-ended sensing degrades severely in ST region due to loss of drive of nMOS and thus reduced read currents.

III. EXISTING 7T SRAM CELL

The architecture of the proposed asymmetric 7T cell is shown in Fig. 2.



F ig.2. Existing 7T SRAM cell

It comprises of an inverter (PUR-PDR) and a pull-up pMOS (PUL), which are coupled together to store one-bit information. An access transistor (ACL) is used for a single-ended write operation and two nMOS (R1, R2) to perform a single-ended read operation. The write bit line (WBL) and write word line (WWL) are used for performing write operations, and the read bit line (RBL) and read word line (RWL) is used for performing a read operation. A nMOS (DL) with its gate terminal connected to ground potential is implemented to provide stability through leakage currents.

A. *Write Ability*

A single-ended write operation is more difficult to perform than the double-ended one in the conventional 6T cell. This is because a conventional 6T cell uses complementary bit lines to perform a write operation and either of the nodes (X or XB) in the cell is discharged quickly through its corresponding bit line. The 7T-C cell accomplishes a write operation through its single bit line, by relying entirely on the mutual effect of inverters to flip the values. Thus, writing ability in the 7T-C cell is achieved by modifying the voltage transfer characteristics

(VTC) of each inverter. The trip point of one inverter is increased while the trip point of the other is decreased.

The conventional 6T SRAM cell is able to maintain write ability down till only 800 mV, while the proposed cell maintains the write margin even at 400 mV. Also, the method of improving write margins for the 7T-C cell by resizing the transistors increases area.

B. Hold State

In the existing cell, as the DL transistor remains in cut off, the X node rises by a small voltage during hold “zero” state, reducing the hold noise margin and making the hold “zero” state more vulnerable. If the X node voltage was to rise beyond the trip point of the PUR-PDR inverter, the cell data would be destroyed. In order to achieve the lowest X node voltage during hold “zero” state, the effective OFF-state resistance from X node to GND must be minimal in comparison to the OFF-state resistance of PUL. This can be achieved by implementing a combination of a wider access transistor (ACL), a longer pull-up transistor (PUL) and an LVT DL.

IV. PROPOSED 7T SRAM CELL

The schemes of the proposed 7T SRAM and the structure of NVSRAM with column-shared technology are shown in fig.3. The proposed AVE-7T1R also utilizes an RRAM with a switch transistor RSWL and two differential power rails. The salient feature of the proposed structure is the additional column-shared virtual switch transistor (SN) connected to the source of the driver transistors (DL and DR), which is area-efficient and in favor of writeability. During the SRAM mode operation, the control signal CTRL of SN is low- and high-voltage level for write and read operations, respectively. As a result, for a write operation, the writeability is significantly improved due to the isolation between the cell core and VSS source. Thus, the stability of R/W will be simultaneously enhanced by using the proposed structure. However, during the write operation, the hold static noise margin (SNM) of the column half-selected cells will be reduced, because they are temporarily isolated with the VSS caused by the low CTRL. Actually, the node VS will be rapidly recovered low state by the selected cell during the write operation, which should be beneficial for the trade off design.

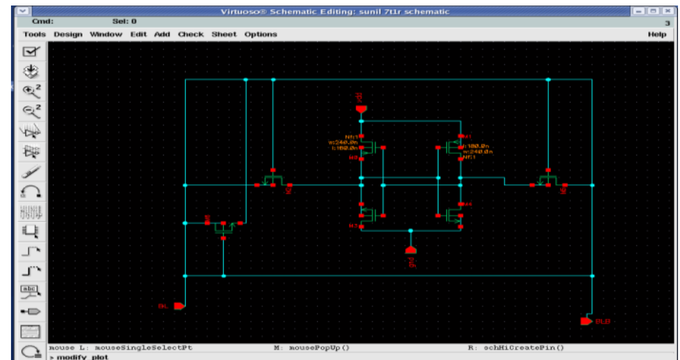


Fig.3. Proposed 7T cell

Simulation Results

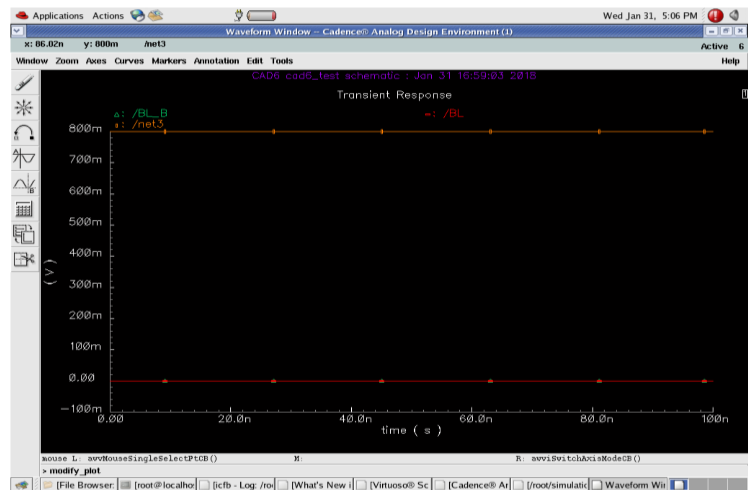


Fig.4.Simulation for conventional 6T SRAM Cell

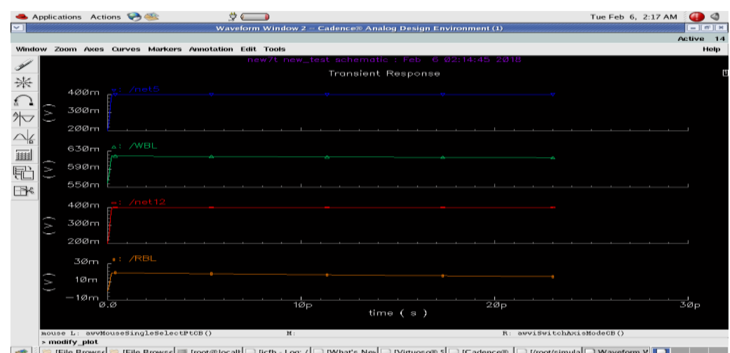


Fig.5. Simulation for Existing 7T SRAM Cell

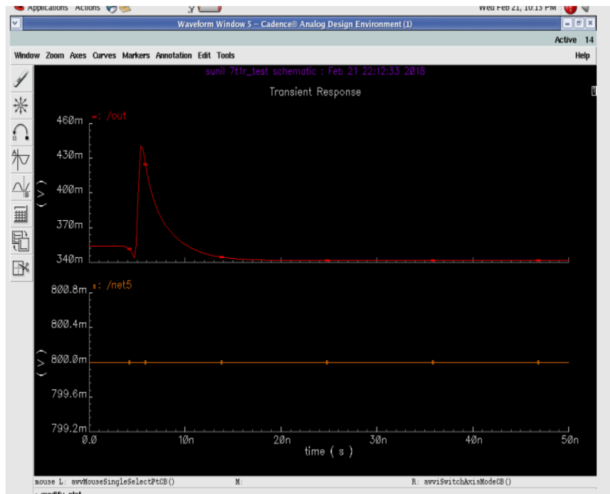


Fig.6. Simulation for proposed 7T SRAM Cell

V. CONCLUSION

In this paper, we propose a new 7T non volatile SRAM cell and it provides the area efficient memory which is used for low power application. It is shown that the proposed circuit shows better read margin (RM) and write margin (WM). The proposed 7T SRAM cell operates in the ST region down to 0.34V. It decreases the area and thereby increasing the performance, the effectiveness of the 7T SRAM cell gives the significant data stability enhancement and leakage power reduction.

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