DESIGN OF HIGH SPEED AND LOW POWER VOLTAGE LEVEL SHIFTER IN DUAL SUPPLY APPLICATIONS

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Abstract

This paper presents an efficient and low-power voltage level shifter for enhanced performance in dual-supply applications. The proposed circuit's efficiency is based on the fact that the strength of the pull-up device is lowered while the pull-down device pulls the output down. At the same time, the pull-down device's strength is increased by an auxiliary circuit that consumes low power. The proposed circuit is simulated in 0.18µm technology Cadence Virtuoso software. The simulation results show that the proposed circuit can convert extremely low level of input voltage into high output voltage level. That is, it can convert low input voltage V_{DDL}=0.8V to high output voltage V_{DDH}=3V with power dissipation of 8.7µW.

Keywords—Voltage Level shifter, low power, Efficiency, power dissipation, voltage range.

I.INTRODUCTION

Static power dissipation and dynamic power dissipation are some sources of power consumption. In digital circuits, we can reduce this static power and dynamic power dissipation by reducing the power supply voltage. But the propagation delay of circuits increases while lowering the power supply voltage. In moderate-speed digital circuits or mixed-signal circuits, some parts operate at high speed; while some parts operate at low speed. In such circuits, instead of reducing the power supply voltage, we can use dual-supply architectures in which two supply voltages are used: low supply voltage (V_{DDL}) and high supply voltage (V_{DDH}). V_{DDL} is supplied for blocks that operate at low speed, i.e., that are in non-crictical paths and (V_{DDH}) is applied for those digital blocks that operate at high speed, i.e., in critical paths. In such a digital system with dual-supply architectures, voltage level shifter circuits are necessary so that they can convert the lower voltage levels into higher voltage levels to provide the needed voltage levels for the next blocks. To enhance the performance of the dual-supply systems, and to avoid the degradation of their performance, the voltage level shifters used should be designed with reduced propagation delay, low power consumption and reduced silicon area. And also to save more power, the voltage level shifters should be capable of converting very low V_{DDL} values to values below the input transistors' threshold voltage. Therefore, in this paper, an efficient and low power voltage level shifter is proposed. This proposed shifter can convert even very low input voltages into high voltages at the output. The remaining of this paper is structured as follows. Analysis of some conventional voltage level shifters in given in Section II. Introduction of the proposed level shifter in Section III. Simulation results of the proposed circuit are presented in Section IV. Lastly, conclusion in Section V.

II. EXISTING SYSTEM

Some of the conventional voltage level shifters are shown in Fig.1. Fig.1a shows a conventional voltage shifter. Its operation is given below. When the input IN is high, i.e., IN=V_{DDL}, the transistor MN1 is ON and pulls down the node Q1; MN2 is OFF. Next, MP2 is slowly turned ON and pulls up the node *Q*2 to V_{DDH} and then turns OFF MP1. Similarly, When the input IN is low, i.e., IN=VSS, the operation is reversed. It is observed that in this circuit, contention is present at the nodes *Q*1 and *Q*2 between the PMOS devices (MP1 and MP2) which are supplied by V_{DDH} and the NMOS devices (MN1 and MN2*)* supplied by V_{DDL}. So, when the difference between V_{DDL} and V_{DDH} is high, and when the input voltage is below the threshold range, this conventional circuit cannot convert the

input voltage levels. Because the currents of the NMOS transistors are smaller than the currents of the PMOS transistors. To overcome this drawback, many attempts have been made. One such approach is to make use of strong PMOS devices by using low threshold transistors and weak NMOS devices by using high threshold transistors[4]. Another attempt is to employ strong NMOS devices by increasing the width of them. This will increase power consumption and also delay. The final approach is to lower the strength

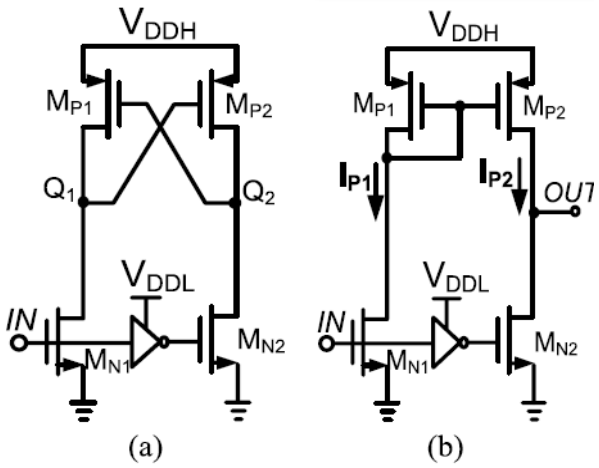

Fig. 1. (a) Conventional voltage level shifter and (b) voltage level shifter with a semi-static current mirror.

of pull-up transistors while the pull-down transistors are pulling the output down [5]–[9]. The circuit shown in Fig. 1(b) employs a semi-static current mirror. It limits the current and this reduces the strength of PMOS transistor (MP2) while the NMOS transistor is pulling down the output. But this circuit has the drawback of static current which flows through MN1 and MP1 when the input signal is high. To reduce this static power consumption, a dynamic current generator may be used. This generator will turn ON at the transition times only[5]–[9].

III. PROPOSED SYSTEM

To overcome the drawback of contention in the existing system, the transition current (IP1 and IP2) should be avoided when the transistor MN2 pulls the output down. This is achieved by the proposed circuit given in Fig.2. Its operation is as follows. When the input goes to HIGH, MN1 turns ON and MN4 turns OFF. MN4 turns ON when OUT does not correspond to input because the overdrive voltage of MP3 is driven by a voltage (i.e., V_{DDH}) larger than that of MN3 (i.e., *V*DDL*)*. Thus, a transition current flows through MP1, MN1 and MN4. This current is mirrored into MP2 and pulls the output node up and MP3 turns OFF. Also, MN4 gate is pulled down which means that there is no static current through MP1, MN1 and MN4. If the aspect ratio of MP1 is chosen smaller than the aspect ratio of MP2, the power consumption can be reduced. During the transition of input signal from high to low, MN2 turns ON and MN1 turns OFF at the same time. Hence, there is no transition current through MP1. Thus, the strength of pull-up device MP2 when the pull-down device pulls the output down. Therefore, the delay, contention and power consumption are reduced. Also, the shifter can correctly work for input voltages in the subthreshold range. This principle is made possible using an auxiliary circuit in the proposed circuit. The auxiliary circuit consists of six transistors MN5.MN6, MN7 and it turn ON only when the input signal changes from high level to low level.

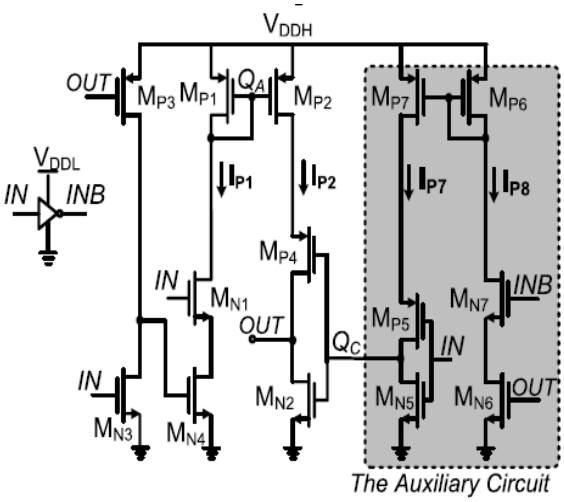

Fig.2. Proposed voltage level shifter.

The auxiliary circuit's operation is as follows. When the input goes low, and when the output does not correspond to input, MN5 turns OFF and MP6, MN6, MN7 are ON. Thus, a transition current will flow through MP6, MN6 and MN7. This current is mirrored into MP7 which pulls the node *QC*. That is MN2 turns ON and MP4 turns OFF and the contention is reduced significantly. When the output is pulled down to ground, MN6 turns OFF and no current is flowing through MP6,MN6 and MN7 which means that the auxiliary circuit is ON only for the transition of the input from high level to low level. Thus the contention is negligible and the propagation delay and power consumption are reduced significantly.

IV. EXPERIMENTAL RESULTS

The proposed level shifter (Fig.2) and conventional level shifters (Fig.1(a) and (b)) have been simulated in Cadence Virtuoso platform in 0.18-μm CMOS

technology. The simulation and experimental results are shown below.

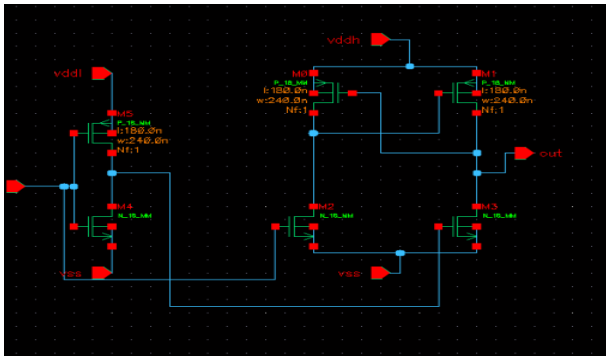

Fig.3. Implementation of schematic of conventional level shifter (Fig.1(a))

In the above-shown level shifter, V_{DDL} of 1.5V and V_{DDH} of 3V are applied and the circuit is simulated in Cadence tool. The simulation result is shown below in Fig.4.

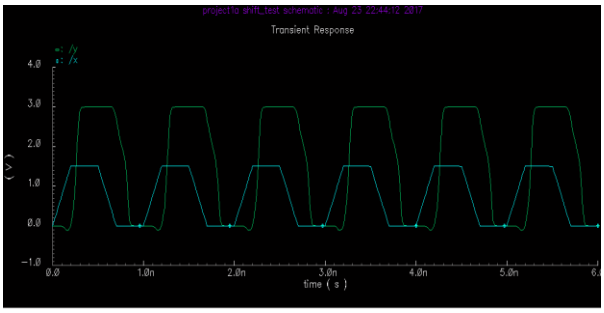

Fig.4. Simulation result of Fig.1(a).

The level shifter with semi-static current mirror shown in Fig.1 (b) is implemented in Cadence tool and shown below.

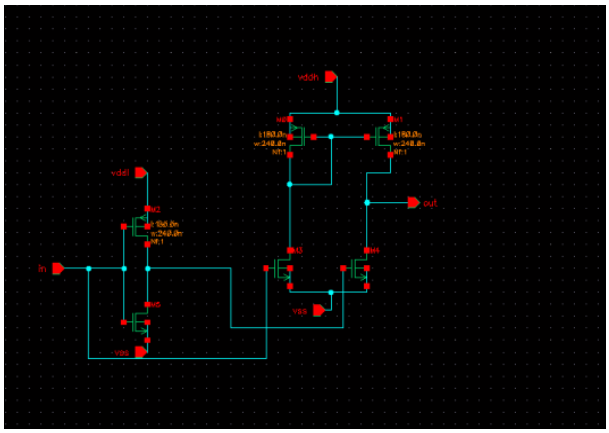

Fig.5. Implementation of schematic of level shifter with current mirror (Fig.1(b)).

For the above circuit, V_{DDL} of 1V and V_{DDH} of 3V are applied and simulated. The simulation result is shown below which shows that it can convert input voltage of 1V to 3V at the output.

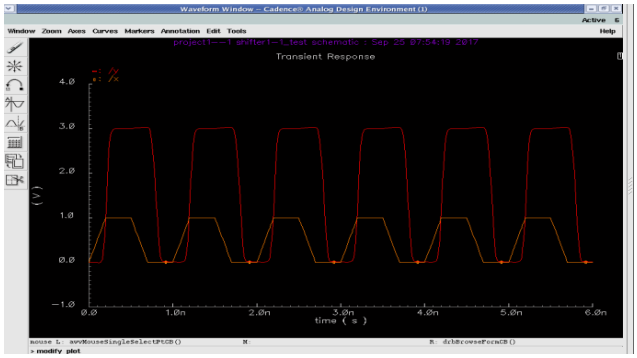

Fig.6. Simulation result of Fig.1(b).

The power consumption of voltage level shifter given in Fig.1(b) is reduced and is lower than that of Fig.1(a). The conventional voltage level shifter (Fig.1(a)) can convert input voltages from 1.5V; it cannot convert input voltage below 1.5V. This is overcome by the level shifter in Fig.1(b) which can convert input voltage of lower than 1.5V.

The proposed level shifter shown in Fig.2 can be able to convert extremely low input voltages also and its simulation is shown below.

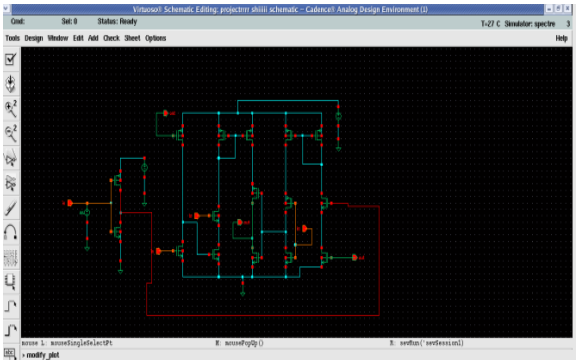

Fig.7. Implementation of schematic of proposed level shifter (Fig.2).

In the proposed level shifter, V_{DDL} value is 0.8V and V_{DDH} value is 3V. The simulation of above circuit shows that the circuit is capable of converting even low input voltage of 0.8V to high output voltage of 3V which is shown below.

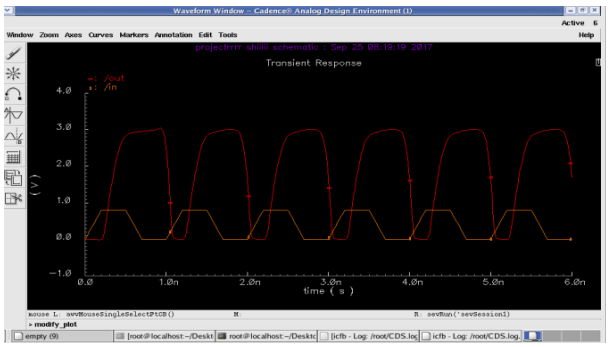

Fig.8. Simulation result of proposed level shifter.

The following table shows the comparison of power consumption of the conventional level shifters and the proposed voltage level shifter.

Table 1. Comparison of simulation results of the conventional and proposed level shifters.

Type	VDDL	VDDH	V_{in}	V_{out}	Power for VDDL=1.5 V
Fig.1(a)	1.5V	3V	1.5 V	3V	453.543µW
Fig.1(b)	1V	3V	1V	3V	63.0609µW
Fig2	0.8V	3V	3V	3V	8.7198 µW

Table I summarizes the power consumption of the structures shown in Fig.1(a), 1(b) and Fig.2. The power consumption of the proposed level shifter is reduced and is lower than the conventional level shifters. Also, the proposed level shifter can convert even extremely low level of input voltages compared to the conventional ones.

V. CONCLUSION

In this paper, an efficient and low-power voltage level-shifter design was proposed. This proposed shifter can convert extremely low level of input voltages. The power consumption of the proposed circuit is also reduced significantly. The simulation and experimental results show that the proposed level shifter is efficient compared to the other existing level shifters.

REFERENCES

[1] A.Wang and A. P. Chandrakasan, "A 180-nm subthreshold FFT processor using a minimum energy design methodology," IEEE *J.* Solid-State Circuits, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[2] K. Usami et al., "Automated low-power technique exploiting multiple supply voltages applied to a media processor," IEEE *J.* Solid-State Circuits, vol. 33, no. 3, pp. 463–472, Mar. 1998.

[3] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for medical implant devices," IEEE *J.* Solid-State Circuits, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.

[4] P. Corsonello, S. Perri, and F. Frustaci, "Exploring well configurations for voltage level converter design in 28 nm UTBB FDSOI technology," in Proc. IEEE Int. Conf. Comput. Design *(*ICCD*)*, Oct. 2015, pp. 499–504.

[5] S. Lütkemeier and U. Ruckert, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," IEEE Trans. Circuits Syst. *II*, Exp. Briefs, vol. 57, no. 9, pp. 721–724, Sep. 2010.

[6] S.-C. Luo, C.-J. Huang, and Y.-H. Chu, "A wide-range level shifter using a modified Wilson current mirror hybrid buffer," IEEE Trans. Circuits Syst. *I*, Reg. Papers, vol. 61, no. 6, pp. 1656–1665, May 2014.

[7] M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," IEEE Trans. Very Large Scale Integr. *(*VLSI*)* Syst., vol. 23, no. 2, pp. 388–391, Feb. 2015.

[8] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "A low-power level shifter with logic error correction for extremely low-voltage digital CMOS LSIs," IEEE *J.* Solid-State Circuits, vol. 47, no. 7, pp. 1776–1783,Jul. 2012.

[9] S. R. Hosseini, M. Saberi, and R. Lotfi, "A low-power subthreshold to above-threshold voltage level shifter," IEEE Trans. Circuits Syst. *II*, Exp. Briefs, vol. 61, no. 10, pp. 753–757, Oct. 2014.

[10] T.-H. Chen, J. Chen, and L. T. Clark, "Subthreshold to above threshold level shifter design," *J.* Low Power Electron., vol. 2, no. 2, pp. 251–258, Aug. 2006.

[11] D. Blaauw and B. Zhai, "Energy efficient design for subthreshold supply voltage

operation," in Proc. IEEE Int. Symp. Circuits Syst., 2006, pp. 4–32.

[12] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, "Sub-Threshold Design for Ultra Low-Power Systems", Secaucus, NJ Springer-Verlag, 2006, ser. Integrated Circuits and Systems.

[13] A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," IEEE *J.* Solid-State Circuits, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[14] S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhandali, T. Austin, D. Sylvester, and D. Blaauw, "Performance and variability optimization strategies in a sub-200 mV, 3.5 pJ/inst, 11 nW subthreshold processor," in Proc. IEEE Symp. VLSI Circuits, Jun. 2007, pp. 152–153.

[15] J. Kwong, Y. K. Ramadass, N. Verma, and A. P. Chandrakasan, "A 65 nm sub-Vt microcontroller with integrated SRAM and switchedcapacitor DC–DC converter," IEEE *J.* Solid-State Circuits, vol. 44, no. 1, pp. 115–126, Jan. 2009.

[16] A. Chavan and E. MacDonald, "Ultra low voltage level shifters to interface sub and super threshold reconfigurable logic cells," in Proc. IEEE Aerosp. Conf., Mar. 2008, pp. 1–6.

[17] I. J. Chang, J.-J. Kim, and K. Roy, "Robust level converter design for sub-threshold logic," in Proc. Int. Symp. Low Power Electron. Design, New York, 2006, pp. 14–19.

[18] A. Hasanbegovic and S. Aunet, "Low-power subthreshold to above threshold level shifter in 90 nm process," in Proc. NORCHIP Conf., Nov. 16–17, 2009, pp 1–4.